Advanced Rules Specifications (Blue Pages)

DOCUMENT IDENTIFIER: A-SP-ELMF030-BP-0000 Rev E, 12-Jul-1991

ABSTRACT: This document provides early planning and prediction information for upcoming improvements in Digital's module process. It also provides a means for feedback exchange and input to the DEC STD 030 committee.

APPLICABILITY: This document provides Digital hardware designers and manufacturing engineers with a preview of future module manufacturing volume process capability, associated design rules, and programs.

STATUS: APPROVED 12-Jul-1991; use VTX SMC for current status.

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REVISION HISTORY:	Rev C,	30-Oct-1989	ECO Number CTS02
	Rev D,	30-Aug-1990	ECO Number CTS03
	Rev E,	12-Jul-1991	ECO Number CTS04

Document Management Category:	Board, Module, and Backplane (HPB)
Responsible Department:	Applied Module/PWB Technology Group (AMPT) A division of the Technical Services for Manufacturing and Engineering Group (TME)
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APPROVAL: This document has been reviewed and approved by the DEC STD 030 Advisory Committee.

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CONTENTS

Preface v

1 MATERIAL CHARACTERISTICS MATRIX 1
1.1 PRE-IMPREGNATED FIBERGLASS CLOTH 1
1.2 CORE OR COPPER CLAD LAMINATES 1
1.3 RESIN 1
1.4 FOIL 1

2 INTRODUCTION AND USE OF METRIC DIMENSIONS — PART 1 4
2.1 ABSTRACT 4
2.2 APPLICATION 4
2.3 GOALS 4
2.4 DEFINITIONS 5
2.5 RULE OF PRECISION 6
2.6 RULE OF EQUIVALENCY 6
2.7 RULE OF DUAL DIMENSIONING 6
2.8 RULE OF METHODOLOGY OR PROCESS 7
2.9 RULE FOR DEFAULT TOLERANCE TABLE 8
2.10 RECOMMENDATION OF IMPLEMENTATION 8
2.11 COST CONSIDERATIONS AND COMPARISONS 9

3 FUTUREBUS+ INTERCONNECT SYSTEM 10
3.1 DEFINITION OF FUTUREBUS+ INTERCONNECT SYSTEM 10
3.2 TYPICAL APPLICATION 10
3.3 PROCESS TIMING 10
3.4 ADVANTAGES 10
3.5 DISADVANTAGES 11
3.6 RELIABILITY 11
3.7 ALTERNATIVES 11
3.8 COST CONSIDERATIONS AND COMPARISONS 11
3.9 FABRICATION REQUIREMENTS AND IMPACTS 12
3.10 TEST REQUIREMENTS AND IMPACTS 13
3.11 ASSEMBLY REQUIREMENTS AND IMPACTS 13
3.12 WORD USE 14
3.13 GENERAL ELECTRICAL DESIGN RULES AND RECOMMENDATIONS 14
3.14 GENERAL MECHANICAL RULES AND RECOMMENDATIONS 17
3.15 TRANSCEIVER RULES and SPECIFICATIONS 17
3.16 VLS RULES AND RECOMMENDATIONS FOR MODULES AND BACKPLANES 18
3.17 PWB/MODULE DESIGN RULES AND RECOMMENDATIONS 23
3.17.1 Routing Density 23
3.17.2 Hole and Pad Sizes 23
3.17.3 Conductor Width and Spacings 24
3.17.4 Layup Drawings 25
3.18 BACKPLANE DESIGN RULES AND RECOMMENDATIONS 26
3.19 CONNECTOR RULES AND RECOMMENDATIONS 27

4 STATUS OF PREVIOUS ADVANCED RULES SPECIFICATIONS 28

Appendix A REFERENCED DOCUMENTS 29

A.1 EL-Class Digital Documents 29

A.2 Other Digital Documents 29

A.3 Other Documents 30

A.4 Ordering Information 30

FIGURES

1 Digital's Bus Value for Option Modules 12

TABLES

1 Properties of Major Resin Systems 2
2 Nominal Copper Thicknesses 3
3 International System of Units 5
4 Table of Metric Hole Size Selections Corresponding to Digital's Standard Requirements in U.S. Customary Units 7
5 Corner Cost Comparisons 11
6 Summary of Component Hole and Signal Via Sizes 24
7 Recommended Line Width 24
8 Suggested Line Widths 25

Preface

Advanced Rules Specifications (Blue Pages)

Advanced Rules Specifications (Blue Pages) provides Digital hardware designers and manufacturing engineers with a preview of future module manufacturing volume process capability, associated design rules, and programs. The development teamwork and strategy represented in this issue reflect the efforts of people working in many groups.

Advanced Rules Specifications (Blue Pages) provides early planning and prediction information for upcoming improvements in Digital's module process. It also provides a means for feedback exchange and input to the DEC STD 030 committee.

DEC STD 030 is the Volume Module Manufacturing Standard. Designs that conform to the DEC STD 030 rule base can expect the highest quality, lowest cost, and, equally important, plant-to-plant transportability with no custom start-up cost or time-to-market delays.

How to Communicate Design Rules

Publishing in the *Blue Pages* is the first formal step in a 3-step process to communicate future design rules and input into Digital's standards. The steps are:

1.	Advanced Rules Specifications (this issue)	Blue Pages	Statement of intent and potential benefits
2.	Proposed Technical and General Reviews	Yellow Pages	Detailed rules
3.	Final Released Standard	White Pages	Final specification

Please review these new design rules against your future needs. Return your questions, comments, and suggestions to Charlie Newall, RUTLND::NEWALL, or to the key contacts listed for the particular subjects in this issue.

For additional copies of this document contact: Charlie Newall, APO-1/D15, DTN: 289-1318, RUTLND::NEWALL.

NOTE

The following design rules are preliminary specifications.

1 MATERIAL CHARACTERISTICS MATRIX

KEY CONTACT

Jim Huff, GSO2/X5, DTN: 354-6202, RAVEN1::HUFF

Technology Overview

The design and manufacture of a printed-wiring board (PWB) uses three major materials: copper foil, woven glass, and resin. The laminator supplies these materials to the PWB manufacturer in the form of pre-impregnated fiberglass cloth (prepregs) and copper-clad laminates.

1.1 PRE-IMPREGNATED FIBERGLASS CLOTH

Prepregs are adhesive sheets used to bond printed-circuit layers together. They are made by impregnating woven glass cloth with a thermoset resin, then carefully controlling the cure advancement of the resin. The properties of the prepreg are critical to the dielectric spacing and circuit encapsulation in the multi-layer board (MLB). Different glass weaves are used to build a MLB. Each weave style absorbs a different volume ratio of resin, and yields a different pressed thickness. These values are usually negotiated between the PWB manufacturer's processing requirements and the laminator's capabilities.

1.2 CORE OR COPPER CLAD LAMINATES

The laminator makes copper-clad laminates according to the PWB manufacturer's specifications. These specifications include nominal thickness, tolerances, construction, grain direction of the glass cloth, size, and copper weight. The construction is important to the dimensional stability, flatness, and ability to drill the laminate.

1.3 RESIN

A thermoset polymer is a resin that goes through a melt region once to cure it. The full cure is reached when the glass transition temperature (Tg) does not increase at increased temperatures. The resin is able to withstand temperatures below its Tg and maintain its physical and electrical properties by absorbing the energy in reorientation within the resin's crystalline structure. If temperatures exceed the Tg of the polymer, the energy is dissipated by decomposition and all mechanical and electrical attributes are dramatically changed. The time and temperature above Tg determine the extent of decomposition. Table 1 lists the major resin systems and their associated properties. Presently available in GSO are general purpose epoxy (FR4), multifunctional FR4, bismaleimide triazine (BT), and polyimide.

1.4 FOIL

Copper foil is made on rolls with one smooth glassy side and one rough nodulated side. The roughened side is called the *treated* side. The treated side promotes a mechanical bond between the resin in the laminate and the copper. Because each resin is different in its bonding capabilities, the copper manufacturer varies the treatments according to the type of resin. Table 2 lists the nominal copper thicknesses offered by the copper manufacturers.

Table 1: Properties of Major Resin Systems†

	General Purpose Epoxy (FR-4)	Multifunctional (MF)	Bismaleimide Triazine (BT)	Polyimide (PI)	Cyanate Ester (CE)
REINFORCEMENT (E or S glass, and so on)	E	E	E	E	E
ELECTRICAL					
Relative dielectrical constant[1] @ 1 MHz	4.5/4.8	4.5/4.8	3.7/4.1	4.4/4.8	3.5/3.8
Volume resistivity after moisture	1.0X10E6	1.5X10E8	N/A	2.9X10E9	1.1X10E12
After elevated temp.	7.0X10E3	6.0X10E7	6.0X10E8	6.2X10E9	1.8X10E13
Electric strength V/mil	975	1175	985	1150	1650
Dissipation factor @ 1 MHz	0.021/0.024	0.018/0.021	0.008/0.014	0.010/0.015	0.009
Arc resistance	118/122	118/121	118	129	160
MECHANICAL					
Glass transition temp. (Tg)'C	120/135	140/150	180/195	220/280	240/260
Coeff. therm. expansion 'C					
Z axis below Tg	60	50	50	55	40
Z axis above Tg	350	300	300	200	270
Peel strength 1 oz. Cu (lbs per in.)	8.0/9.0	6.0/8.0	7.0/8.0	6.5/9.0	7.5/8.5
Flammability	94VO	94VO	94VO	94V0	94VO
Moisture absorption (%)	<0.5	<0.5	<0.5	<1.0	<0.5
CHEMICAL					
Resin content (%)	45/75	47/75	45/75	43/75	43/75
Solvent system	DMF	DMF	DMF/MEK	NMP	DMF
STATUS					
Cost per sq. ft.[2] (Based on FR-4)	$1.0X	$1.2X	$1.7X	$2.1X	$2.0X
Volume availability	Yes	Yes	Yes	Yes	No

[1] For information about effective dielectric constants or material development efforts, contact the key contact person for this paper.

[2] X = The cost of FR-4 standard material. Refer all cost concerns to the key contact person.

† The values shown are given in ranges or in typical values.

Table 1 (Cont.): Properties of Major Resin Systems†

	General Purpose Epoxy (FR-4)	Multifunctional (MF)	Bismaleimide Triazine (BT)	Polyimide (PI)	Cyanate Ester (CE)
Manufacturability[3]	1	2	2	3	3
Business needs[4]	1,2,3	1,3,4	2,4,5	2,4,5,6	2,4,5,6
% used in US	93%	2%	1.4%	3%	<0.5%
Number of laminators supply worldwide	8	5	4	9	4

[3] 1 = Good; no process changes in fabrication.
2 = Fair; some extra bakes and extra process controls.
3 = Poor; no punching, no blanking, no shearing, lamination cure times excessive, drill concerns, extra bakes required and many extra process controls in PWB fabrication and assembly operations.

[4] 1 = <0.093 in. thick
2 = Back panel
3 = Power supplies
4 = Module board
5 = >0.094 in. thick
6 = Repairable
7 = All around use

Table 2: Nominal Copper Thicknesses

Thickness by Weight		Thickness by Gauges		Tolerances	
Oz per sq ft	g per sq m	Nominal in	Nominal mm	In	mm
0.25	76	0.00035	0.009	±0.00003	±0.0008
0.375	114	0.00053	0.013	±0.00005	±0.0013
0.5	153	0.0007	0.018	±0.00007	±0.0018
1.0	305	0.0014	0.035	±0.0001	±0.0025
2.0	610	0.0028	0.071	±0.0003	±0.0076
3.0	915	0.0042	0.106	±0.0004	±0.0102

2 INTRODUCTION AND USE OF METRIC DIMENSIONS — PART 1

KEY CONTACT

Valerie StCyr, LJO1/B1, DTN: 226-2108, BOARDS::STCYR

2.1 ABSTRACT

Digital needs to develop the infrastructure to deliver Futurebus+ compatible products, a metric-based open I/O system, and the ability to readily introduce metric components as they are required for time-to-market competitiveness.

This paper introduces the terms, concepts, and methods for metrication in the design and documentation of Digital's printed-wiring boards (PWBs). The information is consistent with *DEC STD 114-1 Engineering Drawing Requirements - Dimensioning and Tolerancing for Engineering Drawings* and *DEC STD 015-0 Abbreviations and Units of Measurement*.

2.2 APPLICATION

Metric dimensioning has immediate and future applications within Digital. Some of the immediate applications include:

- Futurebus+ card cages/modules
- Dupont Metral 2 mm $\times$ 2 mm edge row connector

Future applications include:

- Use of European documentation standards
- Increased use of metric-dimensioned components such as National/Shinko 0.85 mm pitch SMD and Signetics 0.6 mm pitch SMD.

2.3 GOALS

Both short-term and long-term goals exist for metrication. Short term goals include:

- To increase awareness within Digital's PWB design and manufacturing groups of the need for and results of metrication of PWBs.
- To provide Digital PWB design and manufacturing groups with a common set of terms and concepts.
- To provide the methods for unambiguous design practices that are U.S. customary units and metric equivalent.
- To revise all PWB standards and documents to *hard converted*, dual dimensions.
- To facilitate dual-dimensioning practice.
- To supply PWB design groups with hard metric values. The values for parts designed by Digital should be standard metric, not values unique to Digital.

A long-term goal is to revise all standards, documents, and methods to support metric dimensioning.

2.4 DEFINITIONS

This subhead contains some metric terms and their definitions.

U.S. customary units — The inch-based system. Also known as English; also known as Imperial.

Standard Unit (SU) — 1 SU = 25.0 mm which may be considered one metric *inch*. (Reference: 1 U.S. customary inch = 25.4 mm)

International System of Units (SI) (Le Systeme International d'Unites) — Table 3 shows the multiplication factor, the prefix, and the symbol for common SI prefixes.

Table 3: International System of Units

Multiplication factor			Prefix	Symbol
1 000 000 000 000 000 000	=	10E18	exa	E
1 000 000 000 000 000	=	10E15	peta	P
1 000 000 000 000	=	10E12	tera	T
1 000 000 000	=	10E9	giga	G
1 000 000	=	10E6	mega	M
1 000	=	10E3	kilo	k
100	=	10E2	hecto[1]	h
10	=	10E1	deko[1]	da
0.1	=	10E-1	deci[1]	d
0.01	=	10E-2	centi	c
0.001	=	10E-3	milli	m
0.000 001	=	10E-6	micro	u
0.000 000 001	=	10E-9	nano	n
0.000 000 000 001	=	10E-12	pico	p
0.000 000 000 000 001	=	10E-15	femto	f
0.000 000 000 000 000 001	=	10E-18	atto	a

[1]Avoid using where possible.

Soft Metrication — Maintaining the inch value but expressing it in millimeters is referred to as soft metrication or soft conversion. This is accomplished by multiplying the inch value by 25.4 and expressing the value as millimeters. For example, *DEC STD 176-0 Printed-Wiring Board Acceptance Criteria* lists the minimum conductor width for technology *G* as 0.004 in. *or* 0.10180 mm.

The Institute of Printed Circuits, IPC-MP-83, *Policy on Metrication* states, "There should be no soft conversion merely for the sake of conversion."

Hard Metrication — Replacing the inch value by a reasonable metric value not based on the inch system. For example, the 0.004 in. conductor in the previous example would be 0.10 mm.

IPC-MP-83 states, "While the technique of exact conversion provides good accuracy it will often result in dimensions that are impractical for actual production. For conversions intended for production, it is usually necessary to round to fewer decimal places and apply design judgment to each dimension to assure interchangeability." It also states, "Rationalization will be used to establish preferred metric sizes of items within the spectrum of requirements. These metric sizes will generally be expressed as whole numbers."

2.5 RULE OF PRECISION

The purpose of this rule is to define the required limits of exactitude. Given that interpolations between U.S. customary units and metric will never be equal at the number of significant digits used in board manufacture, no greater precision than the design intent should be introduced by conversion.

DEC STD 015-0 states, "When conversion of units is necessary, the precision of the converted measurement shall reflect the precision of the original measurement." For example, the Dupont Metral connector hole size is 0.75 mm ± 0.08 mm; the U.S. customary conversion should *not* be stated as 0.02952 in. ± 0.00314 in.

2.6 RULE OF EQUIVALENCY

For the purpose of a board's dimensioning, while not strictly equal, the metric and U.S. customary *equivalent* values should be usual and customary in their own base system and should provide parts that are interchangeable. For example, for the connector hole size of 0.75 mm ± 0.08 mm, design judgment is used to determine if the U.S. customary unit equivalent will be:

0.027 in. — 0.032 in. — Fits *inside* the metric window for particularly fit-sensitive designs.
0.026 in. — 0.033 in. — Fits *outside* the metric window to the nearest value at the precision limit.
0.026 in. — 0.031 in. — Shifted lower to eliminate *oversize* condition when slight *undersize* is not a concern.
0.028 in. — 0.033 in. — Shifted higher to eliminate *undersize* condition when slight *oversize* is not a concern.

NOTE

0.027 in. — 0.033 in. was selected as interchangeable with 0.75 mm ±0.08 mm for the Metral solder-in application.

2.7 RULE OF DUAL DIMENSIONING

In dual dimensioning, values and tolerances are expressed in both systems.

According to DEC STD 015-0, subhead 2.2.1 *EEC Requirements* states "Council of the European Communities Directive 80/181/EEC ... requires the use of SI units and certain applicable alternative units as indicated below... There is not a requirement to eliminate non-SI units in dual dimensioning until at least 1999. ... These requirements also apply to products and documents procured from a vendor..."

DEC STD 015-0, subhead 2.2.5 *Dual Units for USA and EEC Products* states, "If a document or product will also be used in the US as well as Europe ... then the US unit should be stated in addition to the SI unit."

"The SI unit should precede the customary unit(s) when two or more units are shown. On drawings, the SI unit should go above the customary unit, as detailed in *DEC STD 114-1 Engineering Drawing Requirements — Dimensioning and Tolerancing for Engineering Drawings.*" For example,
0.75 mm ± 0.08 mm
[0.030 ± 0.003 in.]

2.8 RULE OF METHODOLOGY OR PROCESS

Look-up tables provide the equivalency for common values. Refer to Table 4. Similar tables will be constructed for copper (plated and foils), laminates, laminate tolerances, line widths and spaces, and hole pad codes. Conversion tables eliminate errors for common conversions and standardize the *design judgment* used to derive the hard metric equivalent for common attributes.

Table 4: Table of Metric Hole Size Selections Corresponding to Digital's Standard Requirements in U.S. Customary Units[1]

in	Tolerance	mm	Tolerance
		VIAS	
0.01	+0.003 / -0.01	0.25	+0.08 / - 0.25
0.015	+0.003 / -0.015	0.40	+0.08 / - 0.40
0.02	+0.003 / -0.02	0.50	+0.08 / - 0.50
		COMPONENTS	
0.020	+0.004 / -0.002	0.50	+0.10 / -0.05
0.028	+0.003 / -0.002	0.70	+0.09 / -0.05
0.030	±0.003	0.75	±0.08
0.032	±0.003	0.80	+0.09 / -0.06
0.034	±0.003	0.85	+0.09 / -0.06
0.035	±0.003	0.90	+0.06 / -0.09
0.038	+0.004/-0.003	0.95	+0.12 / -0.06
0.041	+0.002 / -0.003	1.0	+0.04 / -0.08
0.042	+0.005 / -0.003	1.10	+0.09 / -0.11
0.046	±0.004	1.20	+0.07 / -0.13
0.055	±0.004	1.40	±0.10
0.059	±0.004	1.50	±0.10
0.062	±0.004	1.60	±0.10
0.067	±0.005	1.70	±0.13

[1] Unique sizes to be determined as required.

Table 4 (Cont.): Table of Metric Hole Size Selections Corresponding to Digital's Standard Requirements in U.S. Customary Units[1]

in	Tolerance	mm	Tolerance
		COMPONENTS	
0.076	±0.005	1.95	±0.13
0.082	±0.005	2.10	±0.13
0.101	±0.005	2.55	±0.13
0.125	±0.010	3.20	±0.25
		NOT PLATED THROUGH	
0.125	±0.005	3.20	+0.10 / -0.15
0.133	±0.005	3.40	+0.10 / -0.15
0.157	±0.005	4.00	+0.12 / -0.14
0.157	±0.002	4.00	+0.04 / -0.06
0.187	±0.005	4.75	±0.13
0.250	+0/-0.003	6.35	+0/-0.08

NOTE

Standard sizes according to *DEC STD 030-4 Module Manufacturing Standard - Printed-Wiring Board Design Requirements*.
Standard tolerances according to *DEC STD 176-1 Printed-Wiring Board Repair Criteria*.

2.9 RULE FOR DEFAULT TOLERANCE TABLE

Use this rule when dual-dimensioned systems do not incorporate the required tolerance and an equivalency table does not cover the attribute. For example:

in			mm		
.XXX	±	0.010	.XX	±	.25
.XX	±	0.020	.X	±	.50
.X	±	0.100	X.	±	2.50

2.10 RECOMMENDATION OF IMPLEMENTATION

Use the following recommendations for implementation:

- At this time, implementation of metric dimensioning is voluntary.
- For designs choosing to use metric, hard metric shall be used.
- For designs choosing to use metric, dual dimensioning shall be used at this time.
- When the equivalency tables are published in *DEC STD 030-0 Module Manufacturing Standard - Introduction and General Information* the use of those values will be strongly encouraged for purposes of standardization and to eliminate differences in interpretation across Digital and the Digital supply base.

2.11 COST CONSIDERATIONS AND COMPARISONS

The actual cost of producing a design in the dual-dimensioned system of dimensioning and tolerances is the same as the cost of using the U.S. customary system of dimensioning and tolerances.

A design, once converted to dual dimensions according to the related rules and methods, is stable and precise. All PWB manufacturing equipment can be used in either system.

The random conversion of a single-dimensioned design results in confusion and increases the potential for error and resulting scrap.

The universal system will be metric. Until a full metric infrastructure is available within Digital, dual dimensioning bridges the two systems. Dual dimensioning begins the necessary process of learning and converting; cost savings accrue from this standardization.

3 FUTUREBUS+ INTERCONNECT SYSTEM

Key Contacts:

Electrical: Bill Samaras, MLO5-5/E71, DTN 223-7322, ILLBAY::SAMARAS
Mechanical: Dave Moore, MLO11-4/U32, DTN 223-2257, EMDS::MOORE
VLS Design Rules: Bill Braucher BXB1-1/D03, DTN 226-6380, VSSCAD::BRAUCHER
PWB/Module/Backplane Design Rules: Dick Clark, BXB1-1/D03, DTN 293-5189, DANGER::CLARK

Technology Overview

3.1 DEFINITION OF FUTUREBUS+ INTERCONNECT SYSTEM

This technology is a system of elements working together to enhance the complete interconnect between a module (PWB), a connector, and a backplane mounted on a card cage. The total system of interconnect consists of: a backplane with the projecting half of the connector inserted (as a press fit) into through-hole vias; a module (PWB) with the receiving half of the connector inserted (as a press fit) or soldered into through-hole vias, and transceivers mounted on the module to convert the signals for transmission. The primary uses of a Futurebus+ interconnect system are:

- To exchange signals, data, and information between modules in any computing sequence
- To connect power to the modules
- To connect or network systems to each other

3.2 TYPICAL APPLICATION

This system of interconnects is designed to enhance and combine the interface between modules and systems. The bus signals may be implemented using any technology, for example, TTL, ECL, BTL, CMOS, or GaAs as long as the condition of incident-wave switching is maintained on the transmission line signaling environment, with the constraints on skew, crosstalk, and transmission reliability.

3.3 PROCESS TIMING

The Futurebus+ interconnect system is accepted worldwide and is used in all environments. Volume production will be available in Digital in Q4 FY91; prototype and pilot production are available now.

3.4 ADVANTAGES

This system incorporates the working relationships between all electronic elements required for modules or systems to interface with each other. The use of metric dimensioning and tolerances to network with standard elements is cost-effective. The elimination of unique interconnect systems for each Digital product provides additional savings.

The primary advantages to this system are the high rate of data transfer due to the high number of pins available in the connector, the data rate calculation, and the standardized cost.

3.5 DISADVANTAGES

In this system of interconnection, the design engineer must be aware of the cross-talk and reflections that may occur from other modules connected to the same bus. It is not always certain that these conditions are present or that they will inhibit or affect data transfer fidelity, however, the system must be monitored and tested for these conditions.

3.6 RELIABILITY

Exhaustive tests of this technology by many companies yielded more consistent results than any other system used by Digital to date. Refer to IEEE Futurebus+ P896.2, *Physical Layer and Profile Specification*, Draft 5.4, January 18, 1991 (or later), for the detailed reliability test results.

3.7 ALTERNATIVES

Q-bus™, BI™, and XMI™ connector systems using conventional nickel/gold plating and treatment processes with *standard* electrical loses and mechanical process problems are the alternatives. Alternative systems present the fabrication, assembly, and test problems associated with gold plating: repair, handling, insertion, masking for solder, and so on. Futurebus+ technology reduces or eliminates these problems.

3.8 COST CONSIDERATIONS AND COMPARISONS

The primary cost comparisons addressed are between Q-bus, BI, XMI, and Futurebus+ or Futurebus+(Ve). Ve represents value added. Note that the comparison table addresses the *corner* cost; it is the corner of the Futurebus+ module that is key to the Futurebus+ interconnect system. Table 5 shows these comparisons in a very general sense.

Table 5: Corner Cost Comparisons

	Q-bus	BI	XMI	Fbus	Fbus(Ve)
PWB	42	150	310	237	237
Transceivers	59	79	201	90	200
Protocol[1]	—	—	—	274	—
Connector	2	31	31	16	16
Handle	12	—	—	10	10
TOTAL[2]	115	260	542	627	463

[1] Capacitors and components used.

[2] Sum of all parameters listed above.

™ Q-bus, BI, and XMI are trademarks of Digital Equipment Corporation.

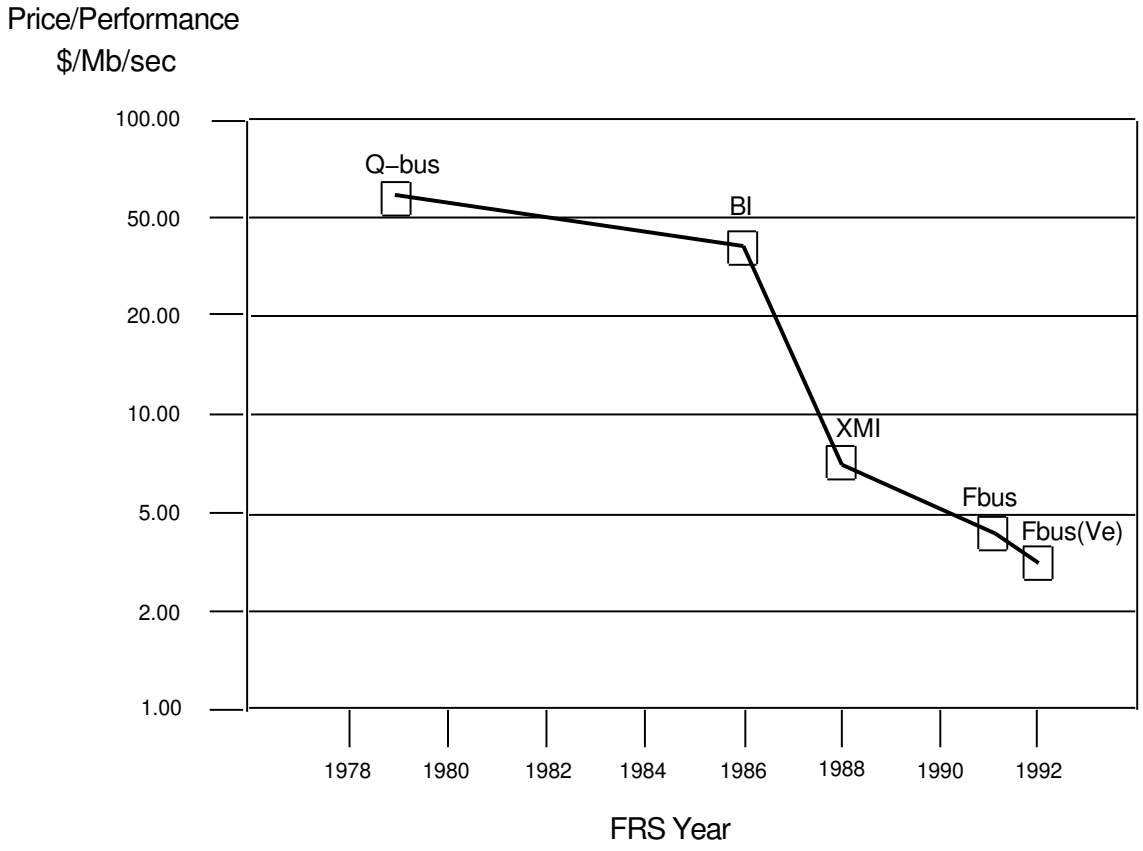
Table 5 (Cont.): Corner Cost Comparisons

	Q-bus	BI	XMI	Fbus	Fbus(Ve)
Bw (Mb/sec)[3]	2	7	80	150	150
FRS	79	86	88	91	91
$/Mb/sec[4]	57.5	37.1	6.78	4.18	3.09

[3]Bandwidth (megabytes/second)

[4]Dollars/mega byte/second

Figure 1: Digital's Bus Value for Option Modules



3.9 FABRICATION REQUIREMENTS AND IMPACTS

Compared to other technologies, the fabrication impact of the PWB and of the backplane is minimal to nonexistent. The reasons for this low impact is that Futurebus+ technology does not require any nickel/gold-plated pads or the processes needed to make those pads, thereby eliminating the problems associated with these processes. Futurebus+ technology does require extra drilled and plated holes for connector pin insertion, but these are standard processes used throughout the PWB industry. For these reasons, the Futurebus+

module and backplane are easier, more cost-effective, and less complicated to build than previous technologies used by Digital.

3.10 TEST REQUIREMENTS AND IMPACTS

The test requirements for bareboard testing do not require additional equipment or processes. Futurebus+ technology actually lends itself to easier, more cost-effective testing because gold pads are not required. Since only through-hole vias for connector prongs, (not fingers), are required, tests are more complete because the entire PWB etch and vias can be probed and tested. In *finger* PWBs, the fingers, or the etch connecting the fingers to the board etch lines, cannot be probed because of possible damage to the soft gold.

3.11 ASSEMBLY REQUIREMENTS AND IMPACTS

Compared to other technologies, the assembly requirements and impacts for this technology are greater than for all other manufacturing processes. Fortunately, not all of these requirements and impacts are negative and, in fact, many are *trade-offs*.

Futurebus+ technology incorporates a connector (half) inserted onto a PWB module, into through-hole vias, heat staked in a *true position* and wave soldered to the PWB. The backplane has the connector mate (half) inserted onto the backplane, into through-hole vias, heat staked in a *true position* and wave soldered to the PWB. This requires special equipment for the true positioning location, staking, clamping to the PWB, and soldering. The trade-offs include that neither a nickel/gold application nor unique tools required for the process are necessary. The connector halves are hand inserted into the module and/or backplane and inspected for proper seating, heat staked in position, and clamped for soldering. All other operations are already in the process.

Refer to drawing B2000, Rev AX19 for assembly dimensions for post assembly use.

Manufacturing Overview

3.12 WORD USE

In the following design rules and recommendations, *shall* indicates a mandatory requirement and *should* indicates a choice.

3.13 GENERAL ELECTRICAL DESIGN RULES AND RECOMMENDATIONS

The following electrical design rules apply. For additional information, refer to the IEEE, P896.2 document.

Signal Integrity

The following rules ensure positive noise margins for Futurebus+ signals when all requirements are met. They include characteristics of the backplane, the module, and the Backplane Transceiver Logic (BTL) transceivers.

Definitions

The following definitions apply:

Zo — Characteristic impedance of signal lines, including connector vias, on the unpopulated backplane.

Zo' — Characteristic impedance of signal lines on backplane populated by male connectors, with termination resistors and no modules inserted.

Rterm — Terminator resistance.

Rsig — Signal etch resistance.

Vterm — Terminator source voltage to be maintained under all load conditions. Vterm is measured from any connector ground pin to the voltage pin on any terminating resistor.

delta_Vgnd — Voltage differential on OV DC rail between any two worst case points of use on the backplane, including terminating resistors and backplane capacitors.

stub — The signal path on the module connecting the BTL transceiver to the Futurebus+ connector.

Zstub — Characteristic impedance of signal line stub on the module.

Lstub — Stub length, measured from the connector via to the center of the transceiver pin surface-mount pad (include etch length from dispersion via, if present).

Conditions for General Rules

Conditions apply to the following general rules.

Slots	Number of slots	14 maximum
Pitch	Module pitch	30 mm
Voltage	+2.1 VAC ripple at any point of use	50 mV maximum
Distribution	Configuration requirement	Partially populated systems shall have plug-in modules distributed as uniformly as possible. Avoid lumping all modules in one area of the backplane.
Vias	Only two per stub	One of the vias may be at the transceiver and the other may be at the connector.
Transceiver	P1194 transceiver	One per stub

- **Rules for Backplane Electrical Characteristics**

  Use the following chart to determine the rules for backplane electrical characteristics.

PARAMETER	VALUE				
Physical:	min	nominal	max	units	Comment
Zo	55		66	ohms	Bare backplane including vias
Zo'	52	57	62	ohms	Connectors, no term. or modules
Rterm		33±1%		ohms	
Rsig			1.0	ohms	
Vterm		2.1±2%		volts	Local bulk and filter capacitance may be required. Refer to P896.2, Section 8.2.7.2.3 for voltage variations.
delta_Vgnd			50	milli-volts	Limits ground-plane voltage drop under maximum current load
Skew			250	pico-sec	Strobe signals should not be slower than corresponding address or data signals.

- **Rules for Module Signal Line Characteristics**

  Use the following chart to determine the rules for module signal line characteristics.

PARAMETER	VALUE				
	min	nominal	max	units	Comment
Zstub	45		75	ohms	
Lstub			25.4	mm	

NOTE

Exceptions to the stub length may be the geographical address lines.

Refer to IEEE, P896.2, for the functional electrical rules concerning:

- Central arbitration signal lines
- Geographical address signal lines
- Module electrical characteristics and design rules
  - Signal skew rules
- Characteristics on transceivers rules
  - Wired-OR glitch filters rules
  - BTL driver rise and fall time rules
  - Transceiver power-on and disabling rules
  - Live insertion feature rules

- **Rule for Resistance**

  All signal lines shall present a resistance, measured from a signal pin on any connector position to the corresponding signal pin on any other connector position of less than 1 ohm. All OV logic pins shall be tied to the OV DC ground plane at their connector pin positions.

- **Rule for Termination**

  Each bus line shall be terminated in a resistance of 36 ohms ±1% to a source of termination voltage at both ends of the backplane. Resistance shall remain within tolerances over all environmental conditions specified in the profile. Surface-mount termination resistors with individual resistor pins for +2.1 V are recommended for lowest inductance, lowest cross-coupling, and better matching to the bus line impedance to minimize reflections.

  The termination circuit shall be capacitively bypassed so the 2.1 V termination voltage, measured at the termination resistors, stays within the limits specified below at all frequencies.

- **Rule for Termination Voltage**

  The termination voltage for all lines on the bus signal paths shall be 2.1 V ± 2%, measured at the termination resistor. This termination voltage may be derived from other voltages available on the backplane, or provided by an external power supply.

3.14 GENERAL MECHANICAL RULES AND RECOMMENDATIONS

The following rules and recommendations apply to the mechanics.

- **Recommendation**

  It is strongly recommended that each module reserve a corner to lay out and place transceivers.

- **Rule for Spacing of Connectors**

  14 connector slots maximum (9 to 10 slots are recommended as normal).

- **Rule for Pitch**

  Module pitch to be 30 mm.

- **Rule for Insertion**

  Insertion force for each module to be approximately 20 to 30 pounds.
  Maximum force to be approximately 50 pounds with all connectors in option.
  Refer to IEEE, P896.2, page 207, for connector-naming conventions and connector assignments.

3.15 TRANSCEIVER RULES and SPECIFICATIONS

In order to alleviate confusion and conform to circumstances of design and purchase, the rules and specifications for transceivers reflect how these devices actually perform. The rules and specifications for Futurebus+ transceivers are being confirmed and must be checked with the Futurebus+ Program Office.

All information is derived from actual silicon measurements. Future changes to the rules and specifications may be made to reflect improvements. At present, the specifications document the worst case for existing silicon designs. These specifications supersede all previous documents.

To obtain these transceiver specifications, access the Fbus notes file (a restricted conference), and read/extract note 113. If you cannot access the notes file and need these specifications, send E-mail to Bill Samaras (ILLBAY::SAMARAS). The specification package is in Digital specification format and is approximately 75 pages long.

The specifications given are:

2030
2031 (points to 2030)
2040
2041
CD3200
3884
3886

Transceiver Vendors

Signetics Inc. is the recommended vendor for transceivers. National Semiconductor Inc. is the secondary vendor. Both semiconductor vendors have agreed with Digital's rules and specifications that are not documented in any other literature.

3.16 VLS RULES AND RECOMMENDATIONS FOR MODULES AND BACKPLANES

The rules and recommendations given here are intended for those familiar with the VLS-oriented CAD process, but not with the B-series of modules, who wish to use the B2999-00 A01 cover package to design Futurebus+ modules.

B2999-00 A01 is a *psuedo Digital part number*, under which heading all files relating to the DEC B2XXX-series of modules may be stored. These files include mechanical drawings, layups, design rules, schematics, and a physical layout that conforms to all of these, as well as the IEEE, P896.2, *Futurebus Profile B*, Section 8.

This file provides a useful starting point plus a path to success in designing Futurebus+ Profile B module options in Digital. No attempt has been made to control B2XXX designs, but B2999 users are provided some protection from inadvertently failing to meet bus requirements.

Where any data item is optional but probable, it has been included for convenience because deleting or changing data is easier than adding it.

Rule of VLS

The core file to any VLS user is the ADS file, which is VLS's archive data structure. The other documents are provided primarily for reference, while the ADS is intended for user modification. This ADS represents many hard decisions by all involved in Profile B.

Constraints:

The following list contains constraints to the VLS rules.

- **Rule for Stub Lengths**

  Implementation of Futurebus+ Profile B modules is heavily constrained by the set of metric intrusive connectors and metric surface mount transceivers selected, plus the limitation to an effective stub length of 25 mm from the backplane to the transceiver pin. For further information, refer to the IEEE, P896.2, Table 8-2.

  Exhaustive studies resulted in a double-sided mixed mount design using a dense via grid, which just barely meets the requirements, with a minimum of PWB and assembly technology required.

- **Rule for Dimensioning**

  Early in the design process, tenths of mils (0.0001 in.) were selected as the design units. Metric units, while most accurate, were found to be a Digital process problem. Mils, on the other hand, are too inaccurate when metric components must be accommodated by a U.S. customary unit data structure.

- **Rule for Hole, Line, Pad, and Spaces**

  The hole, line, pad, and space sizes are nonstandard and are documented in the design rules document. These resulted from trade-off decisions made between design and manufacturing requirements. The minimum conductor-to-conductor space anywhere is about 7 mils.

Additional Information

For further information about these rules or the VALID library, refer to the VALID libraries and schematic database. A component and net TLE (wirelist) of B2999, and seven pages of schematics in VALID form are available. To import the VALID data base and libraries, contact Jim Leahy (CHIRPA::LEAHY) in BXB1.

MSB has agreed to provide the VALID libraries for the Futurebus+ corner design. These libraries include the bodies and part files for all the components used on the corner schematics.

Since these parts and the corner design have not been built and verified, it is possible that the bodies will change. In order to ensure using the latest versions of these files, use DFS to access the directories. When the corner design is approved, it will be placed in a save set available to be copied.

To run DFS, use the command:

RUN SYS$SYSTEM:DFS$CONTROL

at the system level with the logicals assigned so that they are preserved during reboots. The paths are:

DFS> mount .ENG.MSB.LE.CAD.LIBDI
DFS> mount .ENG.MSB.LE.CAD.FLAGD

DFS will create a client divide named DFSCn where n is a VMS™ assigned unit number. The following must be added to STARTUP.GED and COMPILER.CMD:

[deslib.scald.msblib.bodies.fb]fb.lib
[deslib.scald.msblib.bodies.stand]stand.lib
[deslib.scald.msblib.bodies.misc]misc.lib

The connectors are in the stand library. The applicable connectors are conn192 and conn24. The 24-pin connector (conn24) has three versions; version 2 is the power connector and version 3 is the X connector.

The following lines must be added to the PACKAGER.CMD file:

[deslib.scald.msblib.fb]fb.prt
[deslib.scald.msblib.stand]stand.prt
[deslib.scald.msblib.misc]misc.prt

The VALID schematics for the corner are available from the FLAGD DFS logical disk in the following directory:

DANGER::FLAGD:[FLAG.TXXX.R0.GED.T2999]

The schematics consists of seven pages of logic. For further information, contact Brian Parr (CHIRPA::PARR).

Changes:

No cover package can accommodate all the special cases of B-series modules. If the cover data in B2999 is modified prior to designing a Futurebus+ module, bus requirements as specified in P896.2 must be met.

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Most users will not have to make changes. They can import the seven pages of schematics and draw their own additional pages using the same net names as the corner pages where necessary to connect up, generate a wirelist, enter VLS, and use the B2999 ADS file as a VLS cover.

Hints:

Users with special requirements, may consider the following hints.

- **Avoid changing:**
  - The connector and transceiver placement.
  - The physical aspects of the metric part descriptions.
  - The tooling, fiducials, and so on.
  - The stub length of all nets connected to J6, the *B* connector.
  - The hole, pad, and conductor sizes used in B2999.
  - In particular, the dispersion vias done with 15-mil holes (padstacks LVIA, GVIA, PVIA), and the metric connector with 30-mil holes (padstacks CHOL, CHOG, CHOP). For example, if the predominant via size selected elsewhere is 10 or 20 mils, create new padstacks and leave those in the cover alone.
- **Connectors**

  Rules for Connector Use

  B2999 contains 7-metric 4-row intrusive pin connectors, mapped as follows to the control drawing:

  J1=A, J6=B, J4=C, J5=X, J3=D, J7=E, J2=F

  Those not using J7 may delete it. Bridge modules must wire up J7, and generally will have to rewire J5, the central arbitration connector. Deleting or moving any of the J1 to J6 connectors is not recommended.
- **Impedance**

  Recommendation

  An example impedance test strip is provided but may be removed if not needed. If not configured properly for a particular module, the impedance test strip can be reconfigured.

  Rules for Impedance Designs

  The target impedance of BTL in B2999 is 63 ohms. These are routed with conductor code BSIG in the ADS. All other lines (except certain fat etch voltage lines) are to be configured by the user as indicated in the design rules document provided. Their VLS conductor code is CSIG, which is the default for the design as a whole. CSIG is preset for 63 ohms but can be altered in EDIT COVER to suit the particular module's requirement.
- **Bulkhead Mating Holes**

  Rule for Bulkhead Mating Holes

  B2999 includes all bulkhead mating holes in the control drawing, including the optional ones. Those with special cable header requirements may delete or reconfigure these to suit their bulkhead mating scheme. They are P1 to P4.

- **Layups**

  Rules for Layups

  B2XXX modules are permitted to be 10, 8, or 6 layers. B2999 is a 10-layer design, but some of these layers contain no necessary circuitry. It is possible to delete one power plane, (one ground plane in current or voltage drop is not an issue), and two signal layers, if routing is easy. These are purely cost-reduction measures. Layers 2 and 9 are the empty routing layers, while layers 3 and 8 are duplicate GND planes, layers 4 and 7 are duplicate +5 volt planes. Here is what to delete:

B2999	10-layer	8-layer	6-layer
L1	Signal	L1 Signal	L1 Signal
L2	Unused signal	L2 Unused signal	
L3	GND	L3 GND	L2 GND
L4	+5 V		
L5	Signal	L4 Signal	L3 Signal
L6	Signal	L5 Signal	L4 Signal
L7	+5 V	L6 +5 V	L5 +5 V
L8	GND		
L9	Unused signal	L7 Unused signal	
L10	Signal	L8 Signal	L6 Signal

  These layups are specified in D-MD-ELEN646-0-DBU, *Fbus Modules, 6-Layer Construction*, D-MD-ELEN647-0-DBU, *Fbus Modules, 8-Layer Construction* and D-MD-ELEN648-0-DBU, *Fbus Modules, 10-Layer Construction* (all in process). Be sure to adjust the layer names in etch and on sheet one of the MD provided. In addition, a 9-layer layup, D-MD-ELEN649-0-DBU, *Fbus Modules, 9-Layer Construction*, can be used if isolated signal layers are required for signal integrity reasons. To convert from D-MD-ELEN648-0-DBU to D-MD-ELEN649-0-DBU, swap and delete as follows:

B2999	10-layer	9-layer, 2 GND	OR (9-layer), 2 +5 V
L1	Signal	L1 Signal	L1 Signal
L2	Unused signal	L2 Unused signal	L2 Unused signal
L3	GND	L3 GND	L3 GND
L4	+5 V	(Delete)	(Move to L5)
L5	Signal	L4 Signal	L4 Signal
		L5 (Insert L8)	L5 (Insert L4)
L6	Signal	L6 Signal	L6 Signal
L7	+5 V	L7 +5 V	L7 +5 V
L8	GND	(Move to L5)	(Delete)
L9	Unused signal	L8 Unused signal	L8 Unused signal
L10	Signal	L9 Signal	L9 Signal

NOTE

There are additional layups under discussion.

- **Recommendation for Voltage Configuration**

  For those making extensive use of the other Futurebus+ voltages besides GND and +5 V, it will be necessary to reconfigure the power or ground planes. If 3.3 V is used, for example, one option would be to convert L7 to 3.3 V. There are too many different schemes to describe here, but care should be used in any split power plane scheme to avoid the transceiver area.

- **Recommendation for Outlines**

  The module outline is correct for B2XXX modules. When designing B1XXX or B3XXX modules, use the cover provided in B2999, but change the module outline to suit the new requirements.

- **Recommendation for NonFuturebus+ B2XXX Modules**

  B2XXX can be used to design non-Futurebus+ modules, but in that case, the bus interface circuitry may be removed entirely. Be sure to remove the *896* logo — the funny lines forming an 8 out of a 6 and a 9 on layer L10. Also delete the Fbus revision text etch.

- **Other Changes**

  When making other changes, be sure to read all the B2999 reference documents first, as well as P896.2 Section 8. For additional information, send E-mail to TALLIS::BRAUCHER.

3.17 PWB/MODULE DESIGN RULES AND RECOMMENDATIONS

Use the following rules and recommendations for PWB and module designs.

- **Rule for Board Thickness**

  Finished board thickness shall meet the requirements of one of the following layup drawings;

  – 10-layer PWB, D-MD-ELEN648-0-DBU
  – 9-layer PWB, D-MD-ELEN649-0-DBU
  – 8-layer PWB, D-MD-ELEN647-0-DBU
  – 6-layer PWB, D-MD-ELEN646-0-DBU

- **Rule for Board Size**

  The finished board size shall be 289,35 mm [11.392 in.] by 264,85 mm [10.427 in.]. See Circuit Outline Drawing, D-MD-ELEN654-0-DBU, for details.

3.17.1 Routing Density

Use the following rules and recommendations for routing density:

- **Rule for Futurebus+ Corner**

  The design may allow for 1 line between all hole diameters on 1,27 mm [0.050 in.] grid, and 1 line between all hole diameters on 2,00 mm [0.079 in.] grid. The minimum spacing between any two patterns shall be no less than 0,177 mm [0.007 in.].

- **Rule for User Area**

  The design may allow for 2 lines between all hole diameters on 1,27 mm [0.050 in.] grid, and for 2 lines between all hole diameters on 2,54 mm [0.100 in.] grid. The design may allow for 1 line between all hole diameters on 2,00 mm [0.079 in.] grid. The minimum spacing between any two patterns shall be no less than 0,127 mm [0.005 in.].

3.17.2 Hole and Pad Sizes

Use the following rules and recommendations for hole and pad sizes.

- **Rule for Futurebus+ Corner**

  The pad size for holes of 0,381 mm [0.015 in.] diameter shall be 0,76 mm [0.030 in.] on inner layers, and 0,71 mm [0.028 in.] on outer layers (side 1 and 2).

- **Rule for Connector Area**

  The pad size for connector holes of 0,76 mm [0.030 in.] diameter shall be 1,27 mm [0.050 in.] on all layers.

- **Rule for User Area**

  The pad size for hole diameter 1,067 mm [0.042 in.] shall be 1,524 [0.060 in.] on all layers. The pad size for holes of 0,381 mm [0.015 in.] diameter shall be 0,76 mm [0.030 in.] on all layers except L10 (side 2), which shall have 0,889 mm [0.035 in.] pads.

Table 6: Summary of Component Hole and Signal Via Sizes

Feature	PTH Diameter	Pad Diameter	Clearance Size
Hole	0,965 mm to 1,092 mm	1,524 mm	1,778 mm
	[0.038 in. to 0.043 in.]	[0.060 in.]	[0.070 in.]
	0,685 mm to 0,838 mm	1,27 mm	1,524 mm
	[0.027 in. to 0.033 in.]	[0.050 in.]	[0.060 in.]
Via	0,00 mm to 0,406 mm	*See note	1,016 mm
	[0.00 in. to 0.016 in.]		[0.040 in.]

NOTE

Layer 1 shall have 0,711 mm [0.028 in.] pads.
Layers 2,5,6,and 9 shall have 0,76 mm [0.030 in.] pads.
Layer 10 shall have 0,889 mm [0.035 in.] pads.

- **Recommended Board Layup**

  See one of the following drawings for layup requirement:

  10-layer PWB, D-MD-ELEN648-0-DBU
  8-layer PWB, D-MD-ELEN647-0-DBU
  6-layer PWB, D-MD-ELEN646-0-DBU

3.17.3 Conductor Width and Spacings

Use the following rules and recommendations for conductor width and spacing.

- **Rule for Futurebus+ Corner**

  The minimum lateral spacing of internal layer conductors shall be not less than 0,177 mm [0.007 in.]. The minimum lateral spacing of conductors on outer layers (side 1 and side 2) shall be not less than 0,152 mm [0.006 in.].

Table 7: Recommended Line Width

Layer Number	Line Impedance and Width
Side 1	0,203 mm [0.008 in.]
Side 2	0,203 mm [0.008 in.]

- **Rule for User Area**

  The minimum lateral spacing of internal and external layer conductors shall be not less than 0,127 mm [0.005 in.].

  The minimum lateral width of internal and external layer conductors shall be not less than 0,127 mm [0.005 in.].

Table 8: Suggested Line Widths

Layer Number	Line Impedance and Width			
	56 Ohm	60 Ohm	63 Ohm	67 Ohm
L1	0,279 mm	0,228 mm	0,203 mm	0,177 mm
	[0.011 in.]	[0.009 in.]	[0.008 in.]	[0.007 in.]
L2	0,203 mm	0,177 mm	0,152 mm	0,127 mm
	[0.008 in.]	[0.007 in.]	[0.006 in.]	[0.005 in.]
L5	0.203 mm	0.177 mm	0.152 mm	0.127 mm
	[0.008 in.]	[0.007 in.]	[0.006 in.]	[0.005 in.]
L6	0,203 mm	0,177 mm	0,152 mm	0,127 mm
	[0.008 in.]	[0.007 in.]	[0.006 in.]	[0.005 in.]
L9	0,203 mm	0,177 mm	0,152 mm	0,127 mm
	[0.008 in.]	[0.007 in.]	[0.006 in.]	[0.005 in.]
L10	0,279 mm	0,228 mm	0,203 mm	0,177 mm
	[0.011 in.]	[0.009 in.]	[0.008 in.]	[0.007 in.]

- **Rule for HIPOT Test Points**

  Each mutually isolated power or ground plane shall have an identified test point for HIPOT testing.

- **Rule for Soldermasking**

  Use of permanent soldermask coating is required and shall be applied to both sides of the board. Soldermask features (pads) shall be as follows:

  Circuit pad size +0,177 mm [+0.007 in.]. Refer to Table 6.

3.17.4 Layup Drawings

Contact Bill Braucher at TALLIS::BRAUCHER for the postscript files.

3.18 BACKPLANE DESIGN RULES AND RECOMMENDATIONS

For additional information about backplane electrical characteristics, refer to the text under subhead 3.13, in this document. For backplane VLS rules, refer to the text under subhead 3.16 in this document.

Use the following rules and recommendations for backplane designs:

- **Recommendation**

  The backplane is recommended to be 12 layers for present designs. An overall thickness of approximately 2,97 mm [0.117 in.] minimum, 3,63 mm [0.143] maximum is recommended when measured between side 1 and side 2. This design may require a *special* pin length for the connectors selected.

- **Rule for Pad Sizes**

Signal pad size:	1,27 mm or 0.050 in. all layers
Clearance pad sizes:	1,52 mm or 0.060 in. all layers

- **Rule for Line Widths**

  1,27 mm or 0.005 in. exterior layers

- **Rule for Line Spacing** (Signal to any etch)

  0,30 mm or 0.0125 in.

- **Rule for Tolerances**

  Dimensions for dielectric layers apply between copper surfaces. Specified minimum values and toleranced dielectrics must be maintained.

- **Rule for Warp or Twist**

  Maximum warp or twist after fabrication is 0,12 mm per millimeter or [0.005 in. per inch]. Refer to *DEC STD 176-1 Printed-Wiring Board Repair Criteria* for measurement methodology.

- **Rule for Hole Sizes**

	Millimeters	Inches
Finished Hole Size	0,65 - 0,80	0.026 - 0.031
Drilled Hole Size	0,83 - 0,88	0.033 - 0.034
Copper Plating	0,0254 minimum	0.001 minimum
Tin-Lead (fused)	0,004 minimum	0.00015 minimum

- **Rule for Impedance**

  The impedance for all layers shall be 65 ohms ± 10%.

- **Rules for PWB Material**
  - When FR-4 is the base material:
    * Inner-layer copper foil shall meet or exceed Ansi/IPC-CF_150 type ED (electrodeposited).
    * Plated barrel copper shall be 0,0254 mm [0.001 in.] minimum.

    * All electrical requirements of Digital specifications A-PS-1400018-GS and A-PS-1400017-GS must be met.

– When Polyimide is base material:

    * All requirements of Digital specifications A-PS-1400023-GS and A-PS-1400024-GS must be met.

    * Plated barrel copper shall be 0,0254 mm [0.001 in.] minumum.

3.19 CONNECTOR RULES AND RECOMMENDATIONS

Presently, the connector vendor for the Futurebus+ system is Du Pont Inc. using the trade name of Metral. Qualification of additional vendors is expected in July 1991.

Use the following rules and recommendations for connectors:

- **Rule for Connectors**

  Each connector has 2-mm pitch pin-to-pin in four rows of 48 pins.

- **Rule for Signal Pins**

  Each connector (4×6 and 4×48) can have up to 192 pins maximum for signals.

- **Rule for Power/Ground**

  Each connector can have power/ground (pwr/gnd) patterns on pins/blade 207-211 (or 4×2 on 8 connectors).

See the following Purchase Specifications for purchase details:

A-PS-1233430-00, Rev A
A-PS-1233431-00, Rev A
A-PS-1233432-00, Rev A
A-PS-1233433-00, Rev A

4 STATUS OF PREVIOUS ADVANCED RULES SPECIFICATIONS

The following table summarizes the status of specifications included in previous issues of this document.

Title	Key Contact	Status
High Aspect Ratio Drilling (HARD)	Tom Grosskopf	In Advanced Rules Specification of DEC STD 030 (blue pages) issued 30-Mar-1989.
High Aspect Ration Plating (HARP)	Karl Minten	In Advanced Rules Specification of DEC STD 030 (blue pages) issued 30-Mar-1989.
Buried Vias in Multilayer PWB	Jan McCollough	In review (yellow pages).
MCU1	Scott Westbrook	In review for DEC STD 030-11.
HDSC1	Scott Westbrook	In review for DEC STD 030-11.
HPTP	Amalendu Sanyal	In Advanced Rules Specification of DEC STD 030 (blue pages) issued 30-Aug-1990. Will not be included in DEC STD 030.
Controlled Impedance Test Methods	Rich Mellitz	In Advanced Rules Specification of DEC STD 030 (blue pages) issued 30-Aug-1990. Will not be included in DEC STD 030.

APPENDIX A REFERENCED DOCUMENTS

A.1 EL-Class Digital Documents

EL-Class Number	Document Title
EL-00015-00	*DEC STD 015-0 Abbreviations and Units of Measurement*
EL-00030-00	*DEC STD 030-0 Module Manufacturing Standard - Introduction and General Information*
EL-00030-04	*DEC STD 030-4 Module Manufacturing Standard - Printed-Wiring Board Design Requirements*
EL-00114-01	*DEC STD 114-1 Engineering Drawing Requirements - Dimensioning and Tolerancing for Engineering Drawings*
EL-00176-00	*DEC STD 176-0 Printed-Wiring Board Acceptance Criteria*
EL-00176-01	*DEC STD 176-1 Printed-Wiring Board Repair Criteria*

Use VTX SMC to order copies of EL-class documents from Standards and Methods Control. Send distribution questions to JOKUR::SMC or call DTN: 234-4423.

A.2 Other Digital Documents

Document Number	Document Title
A-PS-1233430-00	*Connector, Receptical, Power, Right Angle, 2-mm Grid*
A-PS-1233431-00	*Connector, Receptical, Signal, Right Angle, 2-mm Grid*
A-PS-1233432-00	*Connector, Header, Shrouded, Press Pin, Power, Miniature, 2-mm Grid*
A-PS-1233433-00	*Connector, Header, Shrouded, Press Pin, Signal, Miniature, 2-mm Grid*
A-PS-1400017-GS	*Pre-Impregnated Glass Cloth for PWBs*
A-PS-1400018-GS	*Copper-Clad Thin Laminates for Multi-Signal PWBs*
A-PS-1400023-GS	*Polymide Copper-Clad Laminate for Multilayer PWBs*
A-PS-1400024-GS	*Polymide Pre-Impregnated Glass Cloth (B-Stage) for Multilayer PWBs*
D-MD-ELEN646-0-DBU	*Fbus Modules, 6-Layer Construction*
D-MD-ELEN647-0-DBU	*Fbus Modules, 8-Layer Construction*
D-MD-ELEN648-0-DBU	*Fbus Modules, 10-Layer Construction*
D-MD-ELEN649-0-DBU	*Fbus Modules, 9-Layer Construction*

To receive the referenced design drawings, order A-MN-ELENPCB-02-0, *P.C. Engineering Handbook - Layer Construction Drawings* (in process).

A.3 Other Documents

Document Number	Document Title
IPC-MP-83	*Policy on Metrication*
P896.2	*IEEE, Futurebus+ 896.2, Physical Layer and Profile Specification, Draft 5.4*

A.4 Ordering Information

Following are the sources for documents not available from Standards and Methods Control.

- Purchase specifications are available from the SPOC System or by contacting Sue Haywood at DTN 223-2323.
- Institute of Electrical and Electronic Engineers, Inc.
  345 East 47th St.
  New York, NY 10017, USA
- Institute for Interconnecting and Packaging Electronic Circuits
  7380 N. Lincoln Avenue
  Lincolnwood, IL 60646
  Telephone (708) 677-2850

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